REMARKS

Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

Claims 1, 6, 7, 20 and 21 are currently being amended.

Claim 23 is being added. Support for claim 23 can be found at least in the specification on page 17, paragraph [0027]. No new matter is being added.

This amendment adds and changes claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claim(s) remain under examination in the application, is presented, with an appropriate defined status identifier.

After amending the claims as set forth above, claims 1-23 are now pending in this application, of which claims 2-5, 8-19 and 22 are withdrawn from consideration.

Rejection under 35 U.S.C. § 103

Claims 1, 6, 7, 20 and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,909,151 to Hareland et al. ("Hareland") in view of U.S. Patent Application Publication No. 2002/0011612 to Hieda ("Hieda"). Applicants respectfully traverse this rejection for at least the following reasons.

Independent claim 1, as amended, recites:

> A semiconductor device comprising a protruding semiconductor region formed on a substrate, a protruding source/drain region sandwiching the semiconductor region and a gate electrode formed at least on lateral sides of the semiconductor region via an insulating film,
>
> *wherein the source/drain region has a slope in which at least the largest width is larger than a width of the semiconductor region and the width of the slope continuously increases from the uppermost side to the substrate side in the source/drain region,* and a silicide film is formed on the surface of the slope.

Hareland and Hieda fail to suggest at least the above italicized features of independent claim 1.

The Patent Office, in the bridging paragraph on pages 2-3 of the Office Action, refers to Hareland in FIGs. 3c-8c as disclosing features of claim 1, and specifically equates element 155 of Hareland with the protruding semiconductor region, elements 172/174 of Hareland as the protruding source/drain, and element 160 of Hareland as the gate electrode as recited in claim 1. This rejection is not understood. Hareland does not have FIGs. 3c-8c, nor does Hareland have any of the elements 155, 160, 172 or 174.

Moreover, Hareland does not disclose the recited feature of claim 1 of "wherein the source/drain region has a slope in which at least the largest width is larger than a width of the semiconductor region and the width of the slope continuously increases from the uppermost side to the substrate side in the source/drain region." Hareland discloses a tri-gate transistor 300 in FIGs. 3A and 3B. The Hareland structure includes source and drain regions 330 and 332, and gate 324 over semiconductor body 308. In contrast to claim 1, however, the source and drain regions 330 and 332 are not disclosed as having a slope, much less a slope in which at least the largest width is larger than a width of the semiconductor body 308 (on which the gate 324 is formed), or that the width of the slope continuously increases from the uppermost side to the substrate side in the source/drain region.

Hieda was cited by the Patent Office for disclosing other features of the claims, namely a silicide on its source/drain region 17, but fails to cure the deficiencies of Hareland.

Further, Hareland and Hieda fail to suggest the invention of claim 1 when considered as a whole, where the slope of the source/drain region allows for a silicide film to be formed in a larger area over the source/drain region as compared to a conventional fin-type structure, reducing contact resistance and parasitic resistance (See instant specification, pages 17-18, paragraph [0027]). By contrast, Hareland does not disclose any slope for its source/drain, and Hieda merely discloses a silicide that must be formed on the top of its source/drain due to the insulating sidewalls on the sides of such regions.

The dependent claims under consideration ultimately depend from claim 1, and are patentable for at least the same reasons, as well as for further patentable features recited therein.

Applicants believe that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing or a credit card payment form being unsigned, providing incorrect information resulting in a rejected credit card transaction, or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicants hereby petition for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

Date 7/14/2009

By 

FOLEY & LARDNER LLP
Customer Number: 22428
Telephone: (202) 945-6014
Facsimile: (202) 672-5399

George C. Beck
Attorney for Applicant
Registration No. 38,072

Thomas G. Bilodeau
Attorney for Applicant
Registration No. 43,438